REMARKS

This is intended as a full and complete response to the Final Office Action dated October 18, 2006, having a shortened statutory period for response set to expire on January 18, 2007. Applicants submit this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-22 are pending in the application. Claims 1-22 remain pending following entry of this response. Claims 1, 16, 22 have been amended. Applicants submit that the amendments do not introduce new matter and do not require further search or consideration, as the amendments merely make explicit what was already implicit in the claims.

Examiner Interview

On November 21, 2006, a telephone interview was held between Michael B. McFadden, Examiner and Gero McClellan, Attorney. The parties discussed the claims and potential clarifying amendments to the original claim language. Applicants later sent proposed claim amendments to the Examiner for review. After a review of the proposed claim amendments, the Examiner agreed that the amendments would likely overcome the art of record. However, agreement could not be reached regarding entry of the amendments after final. Since agreement has now been reached regarding the art of record with respect to the amended claims, and since the amendments merely make explicit what was already implicit and what the Applicants had previously argued regarding the meaning of "concatenated," Applicants respectfully request that the amendments be entered and the claims be allowed.

Claim Rejections - 35 U.S.C. § 102

Claims 1-8 and 12-22 are rejected under 35 U.S.C. 102(b) as being anticipated by *Haupt* (US Patent No. 6,334,159). Applicants respectfully traverse this rejection.

In this case, *Haupt* does not disclose "each and every element as set forth in the claim." For example, *Haupt* does not disclose the claim 1, 16 and 22 limitation of "a transfer bus…in the form of a concatenated bus structure…wherein a concatenated bus structure comprises a first point-to-point connection from the memory control device to a first of the one or more memory modules and a second point-to-point connection from the first of the one or more memory modules to a second of the one or more memory modules."

Concatenated is commonly defined as "connected or linked in a series." (See http://dictionary.reference.com/browse/concatenated). Therefore, a concatenated bus structure is one which connects devices to the bus in a series. As Applicants point out in greater detail below, *Haupt* does not disclose a bus structure where devices are connected in series and thus does not disclose a concatenated bus structure.

Haupt is directed to a method and an apparatus for scheduling requests within a data processing system. (*Haupt*, Title) The apparatus of *Haupt* contains a plurality of processing modules 120A each connected to a plurality of memory storage units 110A-D. (See *Haupt*, Figure 2).

The Examiner argues that *Haupt* discloses a concatenated bus structure at Column 5, Lines 40-51. However, the text cited by the Examiner does not describe a concatenated bus structure, rather the cited text describes the functionality of a memory controller.

Furthermore, in contrast to a concatenated bus structure, there are no connections between memory storage units in *Haupt*. (*Haupt*, Figure 2). In contrast, the only connections to memory storage units in *Haupt* are between the processing modules and the memory storage units. (*Haupt*, Column 4, Lines: 64-66). *Haupt* illustrates the interfaces between the processing modules and the memory storage units in Figure 1 as being solely between processing modules and memory storage units. (*Haupt*, Figure 1). Thus, in *Haupt* the processing modules are connected in parallel to the memory storage units. Consequently, *Haupt* does not disclose a concatenated bus structure having a first point-to-point connection from the memory control device to a

first of the one or more memory modules and a second point-to-point connection from the first of the one or more memory modules to a second of the one or more memory modules, rather *Haupt* describes a parallel bus structure.

Therefore, claims 1, 16, 22 and their dependents are believed to be allowable, and allowance of the claims is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

Claims 9, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Haupt* (US Patent No 6,334,159).

Claims 9, 10 and 11 depend from independent claim 1 which is believed to be allowable for the reasons stated above. Therefore, Applicants believe claims 9, 10 and 11 to be allowable for the same reasons, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

If the Examiner believes any issues remain that prevent this application from going to issue, the Examiner is strongly encouraged to contact the undersigned attorney to discuss strategies for moving prosecution forward toward allowance.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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